Docket No.: M4065.0477/P477
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#5/Election
6/25/02
VS

In re Patent Application of:
Kevin M. Devereaux

Application No.: 09/939,636

Group Art Unit: 2815

Filed: August 28, 2001

Examiner: Nguyen, Joseph H.

For: METHOD AND APPARATUS FOR WAFER LEVEL TESTING OF SEMICONDUCTOR USING SACRIFICIAL ON DIE POWER AND GROUND METALIZATION

RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents
Washington, DC 20231

Dear Sir:

In response to the restriction requirement set forth in the Office Action mailed June 4, 2002 (Paper No. 4), Applicant hereby provisionally elects claims 1-8 and 9-11 (Invention I) for continued examination, without traverse.

Dated: June 20, 2002

Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant